**Experiment No. 5**

**Title: Design of digital system using Multiplexer.**

**Batch: B1 Roll No.: 1914078 Experiment No.: 5**

**Aim:** Design of digital system using Multiplexer..

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**Resources needed:** Simulation Platform

**Theory:**

Multiplexer also called Data selector. A digital circuit which selects one of the 2*n* data

inputs and route it to the single output. Select lines are(n) and Input lines are (2n)

.

D0

D1

S0

Q

Input 0

Input 1

Select

Input

fig 1. A 2 : 1 multiplexer

In this case there are two input terminals D0 and D1, one select input S0 and one output Q. When the select input is set to logic 0, D0 is connected to the output. When the select input is set to logic 1, D1 is connected to the output Q.

D0

D1

S1

Q

Input 0

Input 1

Select

Inputs

D2

D3

Input 2

Input 3

S0

fig 2. A 4 : 1 multiplexer.

In this case there are four data input terminals D0 – D3, two select inputs S0 and S1 and just one output Q. The following truth table shows when each of the data inputs is connected to the output.

Table1. Truth table for 4:1 multiplexer

|  |  |  |
| --- | --- | --- |
| **Select Inputs** | | **Output** |
| **S1** | **S0** | **Q** |
| 0 | 0 | D0 |
| 0 | 1 | D1 |
| 1 | 0 | D2 |
| 1 | 1 | D3 |

D0

D1

S1

Q

Input 0

Select

Inputs

D2

D3

Input 7

S0

S2

D4

D5

D6

D7

fig 3. An 8 : 1 multiplexer.

Table 2. Truth Table for 8:1 Multiplexer

|  |  |  |  |
| --- | --- | --- | --- |
| **Selection Inputs** | | | **Output** |
| **S2** | **S1** | **S0** | **Y** |
| 0 | 0 | 0 | D0 |
| 0 | 0 | 1 | D1 |
| 0 | 1 | 0 | D2 |
| 0 | 1 | 1 | D3 |
| 1 | 0 | 0 | D4 |
| 1 | 0 | 1 | D5 |
| 1 | 1 | 0 | D6 |
| 1 | 1 | 1 | D7 |

The above truth table shows when the data inputs are connected to the output.

D0

S1

Q

Input 0

Select

Inputs

S0

S2

D1

D2

D3

D4

D5

D6

D7

S3

D8

D9

D10

D11

D12

D13

D14

D15

Input 15

fig 3. A 16 : 1 multiplexer.

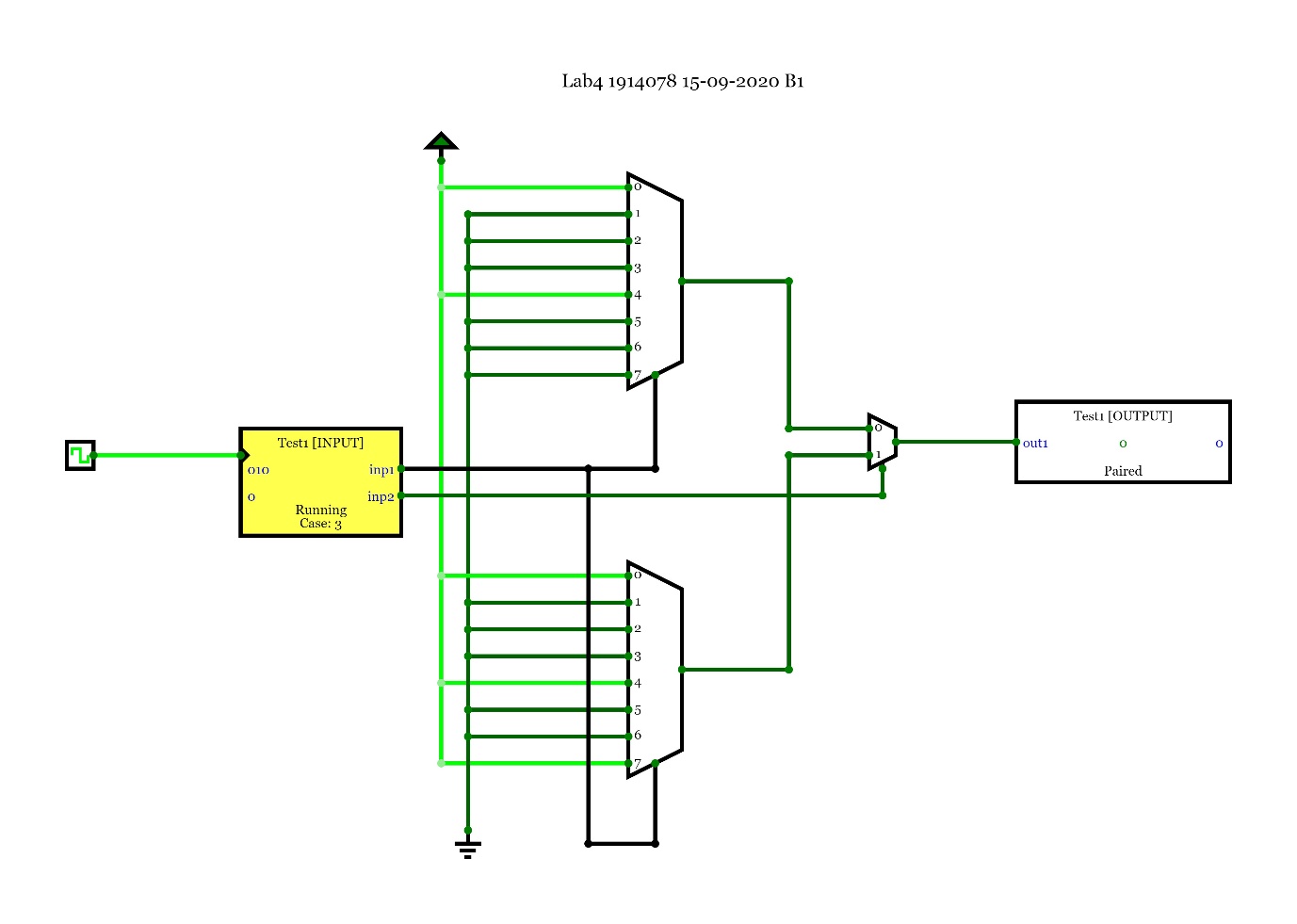
The following truth table shows when the data inputs are connected to the output.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Selection Inputs** | | | | **Output** |
| **S3** | **S2** | **S1** | **S0** | **Y** |
| 0 | 0 | 0 | 0 | D0 |
| 0 | 0 | 0 | 1 | D1 |
| 0 | 0 | 1 | 0 | D2 |
| 0 | 0 | 1 | 1 | D3 |
| 0 | 1 | 0 | 0 | D4 |
| 0 | 1 | 0 | 1 | D5 |
| 0 | 1 | 1 | 0 | D6 |
| 0 | 1 | 1 | 1 | D7 |
| 1 | 0 | 0 | 0 | D8 |
| 1 | 0 | 0 | 1 | D9 |
| 1 | 0 | 1 | 0 | D10 |
| 1 | 0 | 1 | 1 | D11 |
| 1 | 1 | 0 | 0 | D12 |
| 1 | 1 | 0 | 1 | D13 |
| 1 | 1 | 1 | 0 | D14 |
| 1 | 1 | 1 | 1 | D15 |

Multiplexers are commonly used in communication systems; however they can be used in Logic System design and simplification as well. **\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**Procedure**:

1. Design logic circuits for given examples.
2. Simulate the circuit for example 3 and verify the outputs.
3. Upload the write-up with the solved design problems given in write-up.

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Json:-

{"n":16,"inputs":[{"bitWidth":"1","label":"inp1","values":["0","0","0","0","0","0","0","0","1","1","1","1","1","1","1","1"]},{"bitWidth":"3","label":"inp2","values":["000","001","010","011","100","101","110","111","000","001","010","011","100","101","110","111"]}],"outputs":[{"bitWidth":"1","label":"out1","values":["1","0","0","0","1","0","0","0","1","0","0","0","1","0","0","1"]}]}

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**Observations and Results:** Solve the examples as given in write-up/given during Lab session and Simulate as per instructions in Lab session

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**Outcomes:** Design the combinational and sequential circuits using basic building blocks and MSI devices .

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**Conclusion:** We made a design of digital system using Multiplexer.

**Grade: AA / AB / BB / BC / CC / CD /DD**

**Signature of faculty in-charge with date**

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**References:**

**Books/ Journals/ Websites:**

1. R. P. Jain, “Modern Digital Electronics”, Tata McGraw Hill.
2. <http://www.scribd.com/doc/78927750/16-1-Mux-Using-8-1-Mux-4-1mux-And-2-1-Mux#scribd>
3. http://he-coep.virtual-labs.ac.in